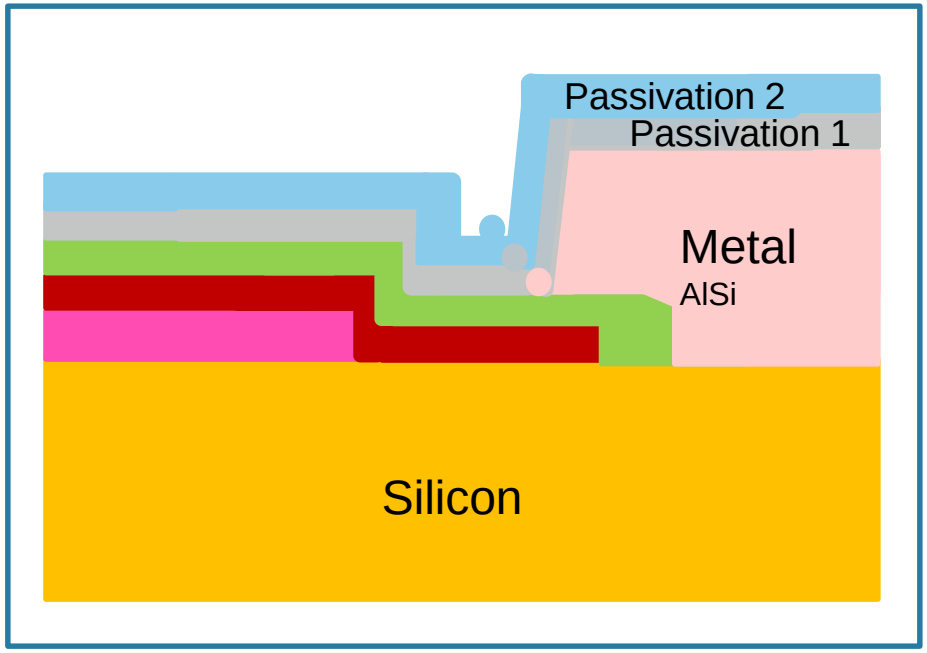
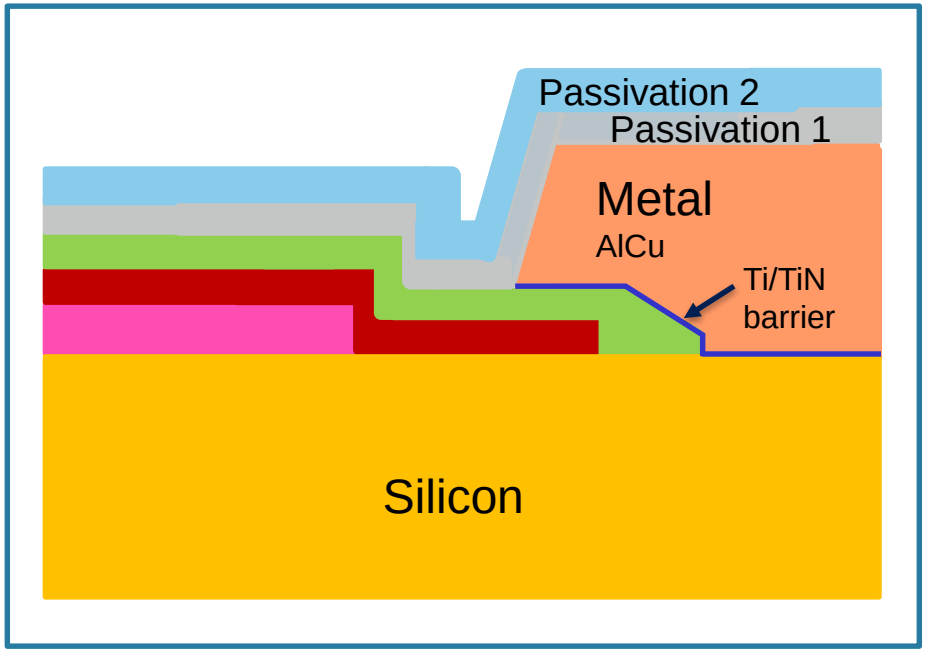
Front Metal Composition
AlCu+Ti/TiN Barrier vs AlSi

Current Structure



New Structure



New Front Metal layer scheme is able to make Metal profile less steep and more regular improving reliability on assembly process.

Catania, December 16th 2018

Automotive Discrete Group (ADG)
Power Transistor Division
HV Business Unit
Process Change Notification

MDmesh™ DM2 Power MOSFET Top Metal change from AlSi to AlCu+Barrier - Ang Mo Kio INDUSTRIAL

Dear Customer,

Following the continuous improvement of our service and in order to improve MDmesh™ DM2 Technology, for selected Power MOSFET Transistors manufactured in ST's Ang Mo Kio (Singapore) FAB, we are going to change the front top metal from AlSi to AlCu+Ti/TiN barrier.

This new process has been developed first on new MDmesh™ DM6 technology and now we are going to apply it also on MDmesh™ DM2.

MDmesh™ DM2 Technology manufactured in Ang Mo Kio (Singapore) FAB, guarantees the same quality and electrical characteristics as per current production.

The involved products series and affected packages are listed in the table below:

Product Family	Technology	Part Number
Power MOSFET Transistors	MDmesh™ DM2	See involved product list

Any other Product related to the above series, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 49-2018.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Test Vehicle
Power MOSFET Transistors	DPAK TO-247 TO-247	STD11N60DM2 STW63N65DM2 STW70N60DM2

Change implementation schedule:

The production start and first shipments will be implemented after week 11 of 2019.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of MDmesh™ DM2, manufactured in ST's Ang Mo Kio (Singapore) FAB with AlCu+Ti/TiN barrier, will be ensured by internal code (Finished Good) and Q.A. number.

Yours faithfully.

Reliability Report
for
MDmesh™ DM2 Power MOSFET
Top Metal change from AlSi to AlCu+Barrier
Ang Mo Kio (Singapore)

Industrial

General Information	
Commercial Product	:STD11N60DM2 - STW63N65DM2- STW70N60DM2
Product Line	: FQ6F01 – FQF901 – FQ6901
Product Description	: MDmesh™ DM2
Package	: DPAK – TO-247
Silicon Technology	: Power MOSFET
Division	: Power Transistor Division

Traceability	
Diffusion Plant	*:* Ang Mo Kio (Singapore)
Assembly Plant	*: Shenzhen (China)*
Reliability Lab	: Catania (Italy)
Reliability Assessment	
Passed	☒
Failed	☐

Disclaimer: *this report is a summary of the qualification plan results performed in good faith by STMicroelectronics to evaluate the electronic devices conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party, except in full, without previous written agreement by STMicroelectronics or under the approval of the author (see below)*

REVISION HISTORY

Version	Date	Author	Changes description
1.0	25 September 2018	A.SETTINIERI	FINAL REPORT

APPROVED BY:
Corrado CAPPELLO
ADG Q&R department - Catania
ST Microelectronics

TABLE OF CONTENTS

1. RELIABILITY EVALUATION OVERVIEW

1.1 Objective

Reliability evaluation for MDmesh™ DM2 Power MOSFET Top Metal change from AlSi to AlCu+Barrier in Ang Mo Kio (Singapore) - INDUSTRIAL

1.2 Reliability Test Plan

Reliability tests performed on this device are in agreement with JESD47 and internal spec 0061692 and are listed in the Test Plan
For details on test conditions, generic data used and spec reference see test results summary at Par.3

TABLE2

#	Stress	Abrv	Reference	Test Flag	Comments
1	Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	Y	
2	External Visual	EV	JESD22B-101	Y	
3	High Temperature Storage Life	HTSL	JESD22B-101	Y	
4	High Temperature Gate Bias	HTGB	JESD22A-108	Y	
5	High Temperature Reverse Bias	HTRB	JESD22A-108	Y	
6	Pre-conditioning	PC	JESD22A-113	Y	
7	Temperature Cycling	TC	JESD22A-104	Y	
8	Autoclave	AC	JESD22A-102	Y	
9	High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	Y	
10	Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	Y	
11	ESD Characterization	ESD (HBM, CDM)	ESDA-JEDEC JES-001 and AINSI-ESD S5.3.1	Y	

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die oriented test showed a good stability of the main electrical monitored parameters.
Package oriented tests have not put in evidence any criticality.
ESD is accordance with ST spec.
On the basis of the overall results obtained, we can give a positive judgment on the reliability evaluation for MDmesh™ DM2 Power MOSFET Top Metal change from AlSi to AlCu+Barrier diffused in Ang Mo Kio (Singapore) and assembled in Shenzhen (China)
In agreement with JESD47 and ST internal spec 0061692

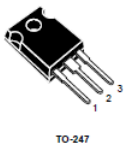
2. DEVICE/TEST VEHICLE CHARACTERISTICS

2.1 Generalities

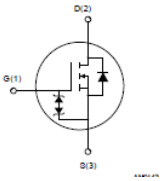
Power MOSFET MDmesh™ DM2

2.2 Pin Connection

DPAK



TO-247



2.3 Traceability

Reference “Product Baseline” document if existing, else provide following chapters/information:

D.U.T.: STD11N60DM2 PACKAGE: DPAK

Wafer fab information	
Wafer fab manufacturing location	SG 6” (Singapore)
Wafer diameter (inches)	6”
Silicon process technology	Power MOSFET - MDmesh™ DM2
Die finishing front side (passivation)	TEOS + Nitride
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	3420 x 2900 µm^2
Metal levels/Materials	AlCu+Ti/TiN barrier

Assembly Information	
Assembly plant location	Shenzhen (China)
Package code description	DPAK
Lead frame/Substrate	TO252 3L (Big Ve5 OpE 30u) / Cu Selected Ni/NiP
Die attach material	PREFORM PbAgSn
Wires bonding materials/diameters	AlMg 5mils (Gate) – Al 10mils (Source)
Molding compound	Halogen Free Molding compound

D.U.T.: STW70N60DM2 PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG 6” (Singapore)
Wafer diameter (inches)	6”
Silicon process technology	Power MOSFET - MDmesh™ DM2
Die finishing front side (passivation)	TEOS + Nitride
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	10390 x 6850 µm^2
Metal levels/Materials	AlCu+Ti/TiN barrier

Assembly Information	
Assembly plant location	Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	TO247 3L (Mon Ve6 OpA/Q) / Cu Selected Ni/NiP
Die attach material	PREFORM PbAgSn
Wires bonding materials/diameters	AlMg 5mils (Gate) – Al 10mils (Source)
Molding compound	Halogen Free Molding compound

D.U.T.: STW63N65DM2 PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG 6” (Singapore)
Wafer diameter (inches)	6”
Silicon process technology	Power MOSFET - MDmesh™ DM2
Die finishing front side (passivation)	TEOS + Nitride
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	10390 x 6850 µm^2
Metal levels/Materials	AlCu+Ti/TiN barrier

Assembly Information	
Assembly plant location	*Shenzhen (China)*
Package code description	TO-247
Lead frame/Substrate	TO247 3L (Mon Ve6 OpA/Q) / Cu Selected Ni/NiP
Die attach material	PREFORM PbAgSn
Wires bonding materials/diameters	AlMg 5mils (Gate) – Al 10mils (Source)
Molding compound	Halogen Free Molding compound

Reliability Testing Information	
Reliability laboratory location	Catania (Italy)
Electrical testing location	Catania (Italy)

3. TESTS RESULTS SUMMARY

3.1 Lot Information

Lot #	Commercial Product	Silicon lines	Package	Wafer Fab	Assembly plant	Note
1	STD11N60DM2	FQ6F	DPAK	SG6”	Shenzhen (China)	
2	STW70N60DM2	FQ69	TO-247			
3	STW63N65DM2	FQF9				

3.2 Test results summary

Test plan results are summarized in the following template.

#	Stress (Abrv)	PC	Std ref.	Conditions	Sample Size (S.S)	Steps	Failure/SS		
							Lot 1	Lot 3	Lot 4
1	**TEST**		User specification	All qualification parts tested per the requirements of the appropriate device specification.			50	190	190
2	**External visual**		JESD22 B-101	All devices submitted for testing			50	190	190
Silicon Oriented Tests									
3	**HTRB**	N	JESD22 A-108	Tj=150°C ; BIAS= 480V	145	1000H	0/45	0/45	
				Tj=150°C ; BIAS= 520V					0/45
4	**HTGB**	N	JESD22 A-108	Tj=150°C ; BIAS= 30V	135	1000H	0/45	0/45	0/45
Die Oriented Tests									
5	**Pre conditioning**		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	All devices to be subjected to H3TRB, TC, AC	Final	Pass		
	TC	Y	JESD22 A-104	TA=-65°C TO 150°C 1 HOURS / CYCLE	75	500cy	0/25	0/25	0/25
6	**AC**	Y	JESD22 A-102	TA=121°C ; PA=2ATM	75	96H	0/25	0/25	0/25
7	**H3TRB**	Y	JESD22 A-101	TA=85°C ; RH=85% BIAS= 100V	75	1000H	0/25	0/25	0/25
8	**IOL**	Y	MIL-STD-750 Method 1037	ΔTj ≥ 100°C	75	10Kcy	0/25	0/25	0/25
9	**ESD**		ESDA–JEDEC JES–001 ANSI – ESD S5.3.1	CDM / HBM	12		0/3 0/3		0/3 0/3